Claims

We claim:

1. An integrated circuit (IC), comprising:

a silicon-on-insulator (SOI) transistor, comprising:

a first source region;

a second source region;

a body contact region, the body contact region electrically coupled to a body region of the silicon-on-insulator (SOI) transistor;

a gate, the gate configured to control a current flow between the first and second source regions and a drain region of the silicon-on-insulator (SOI) transistor;

a first isolation region, the first isolation region disposed between the first source region and the body contact region; and

a second isolation region, the second isolation region disposed between the second source region and the body contact region.

2. The integrated circuit (IC) according to claim 1, further comprising at least one body contact coupled to the body contact region of the silicon-on-insulator (SOI) transistor.

3. The integrated circuit (IC) according to claim 1, wherein the first and second isolation regions comprise dielectric material.

4. The integrated circuit (IC) according to claim 3, wherein the dielectric material comprises silicon dioxide (SiO_2).

5. The integrated circuit (IC) according to claim 3, wherein the dielectric materials comprises silicon carbide (SiC).

6. The integrated circuit (IC) according to claim 1, wherein each of the first and second isolation regions comprises shallow trench isolation (STI).

7. The integrated circuit (IC) according to claim 6, wherein each shallow trench isolation (STI) comprises silicon dioxide (SiO_2).

8. The integrated circuit (IC) according to claim 1, wherein the gate overlaps the body contact region.

9. The integrated circuit (IC) according to claim 1, wherein the body contact region comprises doped semiconductor.

10. The integrated circuit (IC) according to claim 8, wherein the body contact region comprises doped semiconductor.

11. The integrated circuit (IC) according to claim 3, wherein the integrated circuit is a programmable logic device (PLD).

12. The integrated circuit (IC) according to claim 11, wherein the silicon-on-insulator (SOI) transistor resides in a programmable logic circuit within the programmable logic device (PLD).

13. The integrated circuit (IC) according to claim 11, wherein the silicon-on-insulator (SOI) transistor resides in a programmable interconnect within the programmable logic device (PLD).

14. The integrated circuit (IC) according to claim 11, wherein the silicon-on-insulator (SOI) transistor resides in a configuration circuit within the programmable logic device (PLD).

15. The integrated circuit (IC) according to claim 11, wherein the silicon-on-insulator (SOI) transistor resides in a configuration memory within the programmable logic device (PLD).

16. The integrated circuit (IC) according to claim 11, wherein the silicon-on-insulator (SOI) transistor resides in a test/debug circuit within the programmable logic device (PLD).

17. The integrated circuit (IC) according to claim 11, wherein the silicon-on-insulator (SOI) transistor resides in an input/output (I/O) circuit within the programmable logic device (PLD).

18. The integrated circuit (IC) according to claim 11, wherein the silicon-on-insulator (SOI) transistor resides in a test/debug circuit within the programmable logic device (PLD).

19. The integrated circuit (IC) according to claim 11, wherein the silicon-on-insulator (SOI) transistor resides in a processor within the programmable logic device (PLD).

20. The integrated circuit (IC) according to claim 11, wherein the silicon-on-insulator (SOI) transistor resides in a communication circuit within the programmable logic device (PLD).

21. The integrated circuit according to claim 3, wherein the silicon-on-insulator (SOI) transistor resides within an analog circuit.

22. The integrated circuit according to claim 3, wherein the silicon-on-insulator (SOI) transistor resides within a digital circuit.

23. The integrated circuit according to claim 3, wherein the silicon-on-insulator (SOI) transistor resides within a mixed-mode circuit.

24. An integrated circuit (IC), comprising:

a silicon-on-insulator (SOI) transistor, comprising:

a first source region;

a second source region;

a body contact region, the body contact region electrically coupled to a body region of the silicon-on-insulator (SOI) transistor;

a gate, the gate configured to control a current flow between the first and second source regions and a drain region of the silicon-on-insulator (SOI) transistor;

a first extension gate coupled to the gate, the first extension gate disposed adjacent to the body contact region and the first source region; and

a second extension gate coupled to the gate, the second extension gate disposed adjacent to the body contact region and the second source region.

25. The integrated circuit (IC) according to claim 24, further comprising at least one body contact coupled to the body contact region of the silicon-on-insulator (SOI) transistor.

26. The integrated circuit (IC) according to claim 24, further comprising a first semiconductor region disposed between the first source region and the body contact region.

27. The integrated circuit (IC) according to claim 26, further comprising a second semiconductor region disposed between the second source region and the body contact region.

28. The integrated circuit (IC) according to claim 27, wherein the first extension gate is disposed above the first semiconductor region, and wherein the second extension gate is disposed above the second semiconductor region.

29. The integrated circuit (IC) according to claim 28, wherein the first and second semiconductor regions comprise silicon.

30. The integrated circuit (IC) according to claim 24, wherein the gate overlaps the body contact region.

31. The integrated circuit (IC) according to claim 28, wherein the gate overlaps the body contact region.

32. The integrated circuit (IC) according to claim 24, wherein the body contact region comprises doped semiconductor.

33. The integrated circuit (IC) according to claim 31, wherein the body contact region comprises doped semiconductor.

34. The integrated circuit (IC) according to claim 28, wherein the integrated circuit is a programmable logic device (PLD).

35. The integrated circuit (IC) according to claim 34, wherein the silicon-on-insulator (SOI) transistor resides in a programmable logic circuit within the programmable logic device (PLD).

36. The integrated circuit (IC) according to claim 34, wherein the silicon-on-insulator (SOI) transistor resides in a programmable interconnect within the programmable logic device (PLD).

37. The integrated circuit (IC) according to claim 34, wherein the silicon-on-insulator (SOI) transistor resides in a configuration circuit within the programmable logic device (PLD).

38. The integrated circuit (IC) according to claim 34, wherein the silicon-on-insulator (SOI) transistor resides in a configuration memory within the programmable logic device (PLD).

39. The integrated circuit (IC) according to claim 34, wherein the silicon-on-insulator (SOI) transistor resides in a test/debug circuit within the programmable logic device (PLD).

40. The integrated circuit (IC) according to claim 34, wherein the silicon-on-insulator (SOI) transistor resides in an input/output (I/O) circuit within the programmable logic device (PLD).

41. The integrated circuit (IC) according to claim 34, wherein the silicon-on-insulator (SOI) transistor resides in a test/debug circuit within the programmable logic device (PLD).

42. The integrated circuit (IC) according to claim 34, wherein the silicon-on-insulator (SOI) transistor resides in a processor within the programmable logic device (PLD).

43. The integrated circuit (IC) according to claim 34, wherein the silicon-on-insulator (SOI) transistor resides in a communication circuit within the programmable logic device (PLD).

44. The integrated circuit according to claim 28, wherein the silicon-on-insulator (SOI) transistor resides within an analog circuit.

45. The integrated circuit according to claim 28, wherein the silicon-on-insulator (SOI) transistor resides within a digital circuit.

46. The integrated circuit according to claim 28, wherein the silicon-on-insulator (SOI) transistor resides within a mixed-mode circuit.

47. An integrated circuit (IC), comprising:

a transistor, comprising an electro-static discharge (ESD) protection device, the electro-static discharge (ESD) protection device comprising:

a contact coupled to a semiconductor region of the transistor;

a first metal element coupled to the contact;

a via coupled to the first metal element; and

a second metal element coupled to the via.

48. The integrated circuit (IC) according to claim 47, wherein the semiconductor region comprises a drain region of the transistor.

49. The integrated circuit (IC) according to claim 47, wherein the semiconductor region comprises a source region of the transistor.

50. The integrated circuit (IC) according to claim 47, wherein the first metal element comprises a portion of a first metal layer of the integrated circuit (IC).

51. The integrated circuit (IC) according to claim 50, wherein the second metal element comprises a portion of a second metal layer of the integrated circuit (IC).

52. The integrated circuit (IC) according to claim 51, wherein the semiconductor region comprises a drain region of the transistor.

53. The integrated circuit (IC) according to claim 51, wherein the semiconductor region comprises a source region of the transistor.

54. The integrated circuit (IC) according to claim 51, wherein the transistor comprises a silicon-on-insulator (SOI) transistor.

55. The integrated circuit (IC) according to claim 51, wherein the transistor comprises a bulk silicon transistor.

56. The integrated circuit (IC) according to claim 52, wherein the transistor comprises a silicon-on-insulator (SOI) transistor.

57. The integrated circuit (IC) according to claim 52, wherein the transistor comprises a bulk silicon transistor.

58. The integrated circuit (IC) according to claim 51, wherein the integrated circuit is a programmable logic device (PLD).

59. The integrated circuit (IC) according to claim 58, wherein the transistor resides in a programmable logic circuit within the programmable logic device (PLD).

60. The integrated circuit (IC) according to claim 58, wherein the transistor resides in a programmable interconnect circuit within the programmable logic device (PLD).

61. The integrated circuit (IC) according to claim 58, wherein the transistor resides in a configuration circuit within the programmable logic device (PLD).

62. The integrated circuit (IC) according to claim 58, wherein the transistor resides in a configuration memory within the programmable logic device (PLD).

63. The integrated circuit (IC) according to claim 58, wherein the transistor resides in an input/output (I/O) circuit within the programmable logic device (PLD).

64. The integrated circuit (IC) according to claim 58, wherein the transistor resides in a test/debug circuit within the programmable logic device (PLD).

65. The integrated circuit (IC) according to claim 58, wherein the transistor resides in a communication circuit within the programmable logic device (PLD).

66. The integrated circuit (IC) according to claim 58, wherein the transistor resides in a processor within the programmable logic device (PLD).

67. The integrated circuit (IC) according to claim 51, wherein the transistor resides in an analog circuit within the integrated circuit.

68. The integrated circuit (IC) according to claim 51, wherein the transistor resides in a digital circuit within the integrated circuit.

69. The integrated circuit (IC) according to claim 51, wherein the transistor resides in a mixed-mode circuit within the integrated circuit.

70. A method of fabricating a silicon-on-insulator (SOI) transistor in an integrated circuit (IC), the method comprising:

fabricating a first source region of the silicon-on-insulator (SOI) transistor:

fabricating a second source region of the silicon-on-insulator (SOI) transistor:

fabricating a body contact region, the body contact region electrically coupled to a body region of the silicon-on-insulator (SOI) transistor; and

fabricating a gate configured to control a current flow between the first and second source regions and a drain region of the silicon-on-insulator (SOI) transistor;

fabricating a first isolation region, the first isolation region disposed between the first source region and the body contact region; and

fabricating a second isolation region, the second isolation region disposed between the second source region and the body contact region.

71. The method according to claim 70, further comprising fabricating at least one body contact coupled to the body contact region of the silicon-on-insulator (SOI) transistor.

72. The method according to claim 70, wherein fabricating the first and second isolation regions further comprises fabricating the first and second isolation regions from a dielectric material.

73. The method according to claim 72, wherein the dielectric material comprises silicon dioxide (SiO_2).

74. The method according to claim 72, wherein the dielectric materials comprises silicon carbide (SiC).

75. The method according to claim 70, wherein fabricating each of the first and second isolation regions further comprises fabricating a shallow trench isolation (STI).

76. The method according to claim 75, wherein each shallow trench isolation (STI) comprises silicon dioxide (SiO_2).

77. The method according to claim 70, wherein fabricating the gate further comprises overlapping the gate and the body contact region.

78. The method according to claim 70, wherein fabricating the body contact region further comprises fabricating a region of doped semiconductor.

79. The method according to claim 77, wherein fabricating the body contact region further comprises fabricating a region of doped semiconductor.

80. The method according to claim 72, further comprising fabricating the silicon-on-insulator (SOI) transistor in an analog circuit within the integrated circuit (IC).

81. The method according to claim 72, further comprising fabricating the silicon-on-insulator (SOI) transistor in a digital circuit within the integrated circuit (IC).

82. The method according to claim 72, further comprising fabricating the silicon-on-insulator (SOI) transistor in a mixed-mode circuit within the integrated circuit (IC).

83. A method of fabricating a silicon-on-insulator (SOI) transistor in an integrated circuit (IC), the method comprising:

fabricating a first source region of the silicon-on-insulator (SOI) transistor;

a second source region of the silicon-on-insulator (SOI) transistor;

fabricating a body contact region, the body contact region electrically coupled to a body region of the silicon-on-insulator (SOI) transistor;

fabricating a gate configured to control a current flow between the first and second source regions and a drain region of the silicon-on-insulator (SOI) transistor;

fabricating a first extension gate coupled to the gate, the first extension gate disposed adjacent to the body contact region and the first source region; and

fabricating a second extension gate coupled to the gate, the second extension gate disposed adjacent to the body contact region and the second source region.

84. The method according to claim 83, further comprising fabricating at least one body contact coupled to the body contact region of the silicon-on-insulator (SOI) transistor.

85. The method according to claim 83, further comprising fabricating a first semiconductor region between the first source region and the body contact region, wherein the first extension gate is fabricated above the first semiconductor region.

86. The method according to claim 85, further comprising disposing a second semiconductor region between the second source region and the body contact region, wherein the second extension gate is fabricated above the second semiconductor region.

87. The method according to claim 86, wherein the first and second semiconductor regions comprise silicon.

88. The method according to claim 83, wherein fabricating the gate further comprises overlapping the gate and the body contact region.

89. The method according to claim 86, wherein fabricating the gate further comprises overlapping the gate and the body contact region.

90. The method according to claim 83, wherein fabricating the body contact region further comprises fabricating a region of doped semiconductor.

91. The method according to claim 89, wherein fabricating the body contact region further comprises fabricating a region of doped semiconductor.

92. The method according to claim 86, further comprising fabricating the silicon-on-insulator (SOI) transistor in an analog circuit within the integrated circuit (IC).

93. The method according to claim 86, further comprising fabricating the silicon-on-insulator (SOI) transistor in a digital circuit within the integrated circuit (IC).

94. The method according to claim 86, further comprising fabricating the silicon-on-insulator (SOI) transistor in a mixed-mode circuit within the integrated circuit (IC).

95. A method of fabricating a electro-static discharge (ESD) protection device in a transistor in an integrated circuit (IC), the method comprising:

fabricating a contact coupled to a semiconductor region of the transistor;

fabricating a first metal element coupled to the contact;

fabricating a via coupled to the first metal element; and

fabricating a second metal element coupled to the via.

96. The method according to claim 95, wherein the semiconductor region comprises a drain region of the transistor.

97. The method according to claim 95, wherein the semiconductor region comprises a source region of the transistor.

98. The method according to claim 95, wherein the first metal element in fabricating a first metal element coupled to the contact comprises a portion of a first metal layer disposed within the integrated circuit (IC).

99. The method according to claim 98, wherein the second metal element in fabricating a second metal element coupled to the via comprises a portion of a second metal layer disposed within the integrated circuit (IC).

100. The method according to claim 99, wherein the semiconductor region comprises a drain region of the transistor.

101. The method according to claim 99, wherein the semiconductor region comprises a source region of the transistor.

102. The method according to claim 99, wherein the transistor comprises a silicon-on-insulator (SOI) transistor.

103. The method according to claim 99, wherein the transistor comprises a bulk silicon transistor.

104. The method according to claim 99, further comprising fabricating the transistor in an analog circuit within the integrated circuit.

105. The method according to claim 99, further comprising fabricating the transistor in a digital circuit within the integrated circuit.

106. The method according to claim 99, further comprising fabricating the transistor in a mixed-mode circuit within the integrated circuit.